AMENDMENTS TO THE CLAIMS

1. (Previously presented) A magnetic random access memory cell comprising:

a first magnetic storage element having a first sense layer and a first pinned layer;

a second magnetic storage element having a second sense layer and a second pinned layer, said first and second sense layers being mutually electrically coupled through first and second read conductors, said first and second read conductors having respective longitudinal axes, said first and second pinned layers being electrically coupled to respective first and second read/write conductors, said first and second read/write conductors having at least localized longitudinal axes in respective vicinities of said first and second magnetic storage elements, said at least localized longitudinal axes of said first read/write conductor being oriented substantially parallel to said longitudinal axis of said first read conductor;

a switching device coupled to said mutually coupled pinned layers through said first and second read conductors and configured to couple said mutually coupled pinned layers to a conductor for receiving a substantially constant potential.

2. (Previously presented) A magnetic random access memory cell as defined in claim 1 wherein said substantially constant potential comprises a ground potential.

3. (Previously presented) A magnetic random access memory cell as defined in claim 1 wherein said first magnetic storage element and said second magnetic storage element are disposed above said switching device in a first direction, and wherein said switching device is disposed adjacent to a second switching device of a second magnetic random access memory cell.

4. (Previously presented) A memory device comprising:

a plurality of read/write conductors respectively paired with a plurality of read conductors, said respectively paired read/write and read conductors having substantially parallel longitudinal axes;

at least one memory cell electrically coupled to each said respectively paired read/write conductor and read conductor, said at least one memory cell including a transistor and two resistive memory elements, said two resistive memory elements being electrically connected in series by respective said read conductors, said two resistive memory elements being mutually coupled to said transistor at a common node.

5. (Previously presented) A memory device as defined in claim 4 wherein:

said two resistive memory elements each include a pinned layer and a sense layer; and

wherein said sense layer of each said resistive memory element is electrically coupled through said transistor to a conductor for receiving a substantially constant electrical potential.

6. (Previously presented) A memory device as in claim 5 wherein said substantially constant electrical potential is a ground potential.

7. (Previously presented) A memory device as defined in claim 4 wherein said transistor comprises:

two transistors having a common drain connection and respective gate terminals, said gate terminals mutually coupled to one another.

8. (Previously presented) A memory device as defined in claim 4 wherein:

said first and second resistive memory elements are disposed in layered spaced relation to one another above said transistor.

9. (Previously presented) A memory device as defined in claim 4 further comprising:

a word line conductor electrically coupled to a gate of said transistor.

10. (Original) A memory integrated circuit comprising:

a first two-dimensional array of resistive memory elements disposed in substantially parallel spaced relation between a second two-dimensional array of resistive memory elements and a third two-dimensional array of isolation devices, each isolation device of said third two-dimensional array being coupled to at least one resistive memory element of said first two-dimensional array and at least another resistive memory element of said second two-dimensional array;

a first plurality of read/write conductors having respective longitudinal axes oriented in a first direction and coupled to said first two-dimensional array of resistive memory elements; and

a second plurality of read conductors having respective longitudinal axes also oriented in said first direction and also coupled to said first two-dimensional array of resistive memory elements.

11. (Original) A memory integrated circuit as defined in claim 10 wherein said first array of resistive memory elements comprises an array of MRAM memory elements.

12. (Previously presented) A memory integrated circuit as defined in claim 10 wherein said first array of resistive memory elements comprises an array of programmable conductive memory elements.

13. (Original) A memory integrated circuit as defined in claim 10 further comprising:

a sensing circuit, said sensing circuit adapted to sense a state of said resistive memory elements during a time interval when a respective isolation device is activated.

14. (Original) A memory integrated circuit comprising:

a plurality of memory cells, each cell including:

first and second resistive memory storage elements, said first and second resistive memory storage elements being electrically coupled to respective first and second memory sensing circuits, said first and second resistive memory storage elements being mutually coupled to a reference potential through a common dual transistor.

15. (Original) A memory integrated circuit as defined in claim 14 wherein said first and second resistive memory storage elements are disposed in spaced relation above said common dual transistor.

16. (Original) A memory integrated circuit as defined in claim 14 further comprising an address decoder electrically coupled to first and second gates of said dual transistor and adapted to activate said dual transistor in response to an address signal received at an address input of said address decoder.

17. (Previously presented) A magnetic random access memory device comprising:

a semiconductor substrate having an upper surface;

a transistor having a drain region supported by said semiconductor substrate;

a first magnetic random access memory storage element over said upper surface and above said drain region and electrically coupled to said drain region through a first read conductor, said first read conductor having a first longitudinal axis;

a second magnetic random access memory storage element over said upper surface and above said first magnetic random access memory storage element and electrically coupled to said first magnetic random access memory storage element and said drain region through a second read conductor, said second read conductor having a second longitudinal axis; and

first and second read/write conductors having respective third and fourth longitudinal axes, said first longitudinal axis being disposed substantially parallel to said third longitudinal axis, said second longitudinal axis being disposed substantially parallel to said fourth longitudinal axis.

18. (Previously presented) A programmable conductive memory device comprising:

a semiconductor substrate having an upper surface;

a transistor having a drain region supported by said semiconductor substrate;

a first programmable conductive memory storage element disposed above said upper surface and electrically coupled to said drain region by a first read conductor, said first read conductor having a first longitudinal axis;

a second programmable conductive memory storage element disposed above said first programmable conductive memory storage element and electrically coupled to said first programmable conductive memory storage element and said drain region through a second read conductor, said second read conductor having a second longitudinal axis; and

first and second read/write conductors having respective third and fourth longitudinal axes, said first longitudinal axis being disposed substantially parallel to said third longitudinal axis, and said second longitudinal axis being disposed substantially parallel to said fourth longitudinal axis.

19. (Previously presented) A method of manufacturing a digital data storage device comprising:

forming a transistor layer, including a plurality of transistors, over a semiconductor substrate;

forming a first resistive memory storage layer over said transistor layer, said first resistive memory storage layer comprising a plurality of first resistive memory storage structures, each of said plurality of first resistive memory storage structures including respectively paired read conductors and read/write conductors, wherein said read conductors and said read/write conductors each have a respective longitudinal axis and said longitudinal axes of said respectively paired read conductors and read/write conductors are disposed in a substantially parallel relationship;

forming a second magnetic memory storage layer over said first magnetic memory storage layer, said second magnetic memory storage layer comprising a plurality of second magnetic memory storage structures; and

electrically coupling respective ones of said plurality of transistors, said plurality of first magnetic memory storage structures, and said plurality of second magnetic memory storage structures.

20. (Previously presented) A method of manufacturing a digital data storage device as defined in claim 19 further comprising forming a control circuit over said semiconductor substrate, said control circuit being configured for activating said plurality of transistors.

21. (Currently amended) A processing system comprising:

a plurality of memory cells, each cell including:

first and second resistive memory storage elements, said first and second resistive memory storage elements being electrically coupled to respective first and second memory sensing circuits, said first and second resistive memory storage elements being mutually coupled to a reference potential through a wired-NOR FLASH memory [[style]] transistor.

22. (Currently amended) A method of forming a memory device comprising:

forming a plurality of NOR FLASH-memory [[style]] transistors disposed in an array over a semiconductor substrate;

forming an array of first resistive memory elements over said transistors;

forming an array of second resistive memory elements over said first resistive memory elements; and

electrically coupling at least one second resistive memory element to a respective first resistive memory element and to a respective transistor.